AMENDMENTS TO THE CLAIMS

Claims 1-43 are pending in the instant application. Claims 20-27 have been cancelled. Claims 1, 9, 15, 28, 34 and 38 are independent. Claims 2-8, 10-14, 16-19, 29-33, 35-37 and 39-43 depend from independent claims 1, 9, 15, 28, 34 and 38, respectively.

Listing of claims:

1. (Previously Presented) A multi-mode wireless communication device, comprising:

a host baseband processor configured to operate in accordance with a first wireless communications protocol of a first wireless communications system; and

a baseband co-processor configured to operate in accordance with a second wireless communications protocol of a second wireless communications system,

wherein said host baseband processor is operable to time synchronize said second wireless communications system to said first wireless communications system based on timing information transferred to said host baseband processor from said baseband co-processor.

2. (Previously Presented) The multi-mode communications device of claim 1, wherein said host baseband processor comprises circuitry for issuing, from said host

baseband processor, a timer capture interrupt to said baseband co-processor during a predetermined timer phase of said first wireless communications system.

3. (Previously Presented) The multi-mode communication device of claim 2, wherein said baseband co-processor is configured to provide at least one timer value pertinent to a timing state of said second wireless communications system to said host baseband processor in response to issuance of said timer capture interrupt, said host baseband processor enables determining of a timing difference between said first and second wireless communication systems based upon said predetermined timer phase and said at least one timer value.

4. (Previously Presented) The multi-mode communications device of claim 1, wherein said host baseband processor comprises circuitry for reading a current value of at least one timer maintained by said baseband co-processor consistent with said second wireless communications protocol.

5. (Previously Presented) The multi-mode communications device of claim 1, wherein said host baseband processor comprises a higher-layer processing module and a modem for interfacing with said first wireless communication system, said higher-layer processing module being operatively coupled to said modem and to a baseband interface of said baseband co-processor.

6. (Previously Presented) The multi-mode communications device of claim 3, wherein said second wireless communications protocol comprises WCDMA, said baseband co-processor including first and second registers adapted to store said at least one timer value and an additional timer value pertinent to said second wireless communications protocol.

7. (Previously Presented) The multi-mode communications device of claim 6, wherein said at least one timer value corresponds to a slot counter and said additional timer value corresponds to a sample counter.

8. (Previously Presented) The multi-mode communications device of claim 1, wherein said host baseband processor comprises a higher-layer processor configured to effect higher-layer processing of information processed by said baseband co-processor.

9. (Previously Presented) A timing synchronization method, comprising:

configuring a host baseband processor of a multi-mode device to operate in accordance with a first wireless communications protocol of a first wireless communications system;

configuring a baseband co-processor of a multi-mode device to operate in accordance with a second wireless communications protocol of a second wireless communications system; and

establishing, by said host baseband processor within said device, timing synchronization of said second wireless communication system to said first wireless communications system based on timing information transferred to said host baseband processor from said baseband co-processor.

10. (Previously Presented) The method of claim 9, wherein said establishing includes issuing a timer capture interrupt to said baseband co-processor.

11. (Previously Presented) The method of claim 10, wherein said establishing comprises providing at least one timer value pertinent to a timing state of said second wireless communications system to said host baseband processor in response to issuance of said timer capture interrupt.

12. (Previously Presented) The method of claim 9, wherein said establishing includes reading a current value of at least one timer maintained by said baseband co-processor consistent with said second wireless communications protocol.

13. (Previously Presented) The method of claim 11, wherein said second wireless communications protocol comprises WCDMA, said establishing including storing at least one timer value and an additional timer value pertinent to an additional timing state of said second wireless communications system in first and second registers of said baseband co-processor.

14. (Previously Presented) The method of claim 9, wherein said host baseband processor is configured to effect higher-layer processing of information processed by said baseband co-processor.

15. (Previously Presented) A method for wireless communication, the method comprising:

generating by a host baseband processor within a multi-mode communication device, a timer capture interrupt during a predetermined timing phase of a first wireless communication system, wherein said host baseband processor within said multi-mode communication device communicates via a first wireless protocol with said first wireless communication system, and wherein a baseband co-processor within_said multi-mode communication device communicates via a second wireless protocol with a second wireless communication system;

receiving by said host baseband processor from said baseband co-processor, a timer value of at least one timing state pertinent to operation of said second wireless

communication system in response to said baseband co-processor receiving said generated timer capture interrupt;

storing and/or reading said timer value; and

determining by said host baseband processor a timing relationship for synchronizing said second wireless communication system to said first wireless communication system, based upon said received timer value from said baseband co-processor.

16. (Previously Presented) The method of claim 15, comprising:

storing an additional timer value of at least one other timer pertinent to operation of said second wireless communication system in response to said timer capture interrupt; and

reading said additional timer value, said timing relationship being based at least in part upon said additional timer value.

17. (Previously Presented) The method of claim 15, wherein one or more timers are incremented pursuant to operation of said first wireless communication system, said determining a timing relationship including comparing at least one value of said one or more timers with said timer value.

18. (Previously Presented) The method of claim 15, wherein said first wireless communications system operates in accordance with a first wireless communications protocol, and said second wireless communications system operates in accordance with a second wireless communications protocol different from said first wireless communications protocol.

19. (Previously Presented) The method of claim 18, wherein said first wireless communications protocol comprises GSM, and said second wireless communications protocol comprises WCDMA.

20 -27. (Cancelled)

28. (Previously Presented) A multi-mode wireless communication device, comprising:

a host baseband processor configured to operate in accordance with a first wireless communications protocol of a first wireless communications system; and

a baseband co-processor configured to operate in accordance with a second wireless communications protocol of a second wireless communications system,

wherein said host baseband processor is operable to time synchronize said second wireless communications system to said first wireless communications system based on timing information transferred to said host baseband processor from said

baseband co-processor, wherein said host baseband processor comprises circuitry for issuing, from said host baseband processor, a timer capture interrupt to said baseband co-processor during a predetermined timer phase of said first wireless communications system, and wherein said baseband co-processor is configured to provide at least one timer value pertinent to a timing state of said second wireless communications system to said host baseband processor in response to issuance of said timer capture interrupt, said host baseband processor enables determining of a timing difference between said first and second wireless communication systems based upon said predetermined timer phase and said at least one timer value.

29. (Previously Presented) The multi-mode communications device of claim 28, wherein said host baseband processor comprises circuitry for reading a current value of at least one timer maintained by said baseband co-processor consistent with said second wireless communications protocol.

30. (Previously Presented) The multi-mode communications device of claim 28, wherein said host baseband processor comprises a higher-layer processing module and a modem for interfacing with said first wireless communication system, said higher-layer processing module being operatively coupled to said modem and to a baseband interface of said baseband co-processor.

31. (Previously Presented) The multi-mode communications device of claim 28, wherein said second wireless communications protocol comprises WCDMA, said baseband co-processor including first and second registers adapted to store said at least one timer value and an additional timer value pertinent to said second wireless communications protocol.

32. (Previously Presented) The multi-mode communications device of claim 31, wherein said at least one timer value corresponds to a slot counter and said additional timer value corresponds to a sample counter.

33. (Previously Presented) The multi-mode communications device of claim 28, wherein said host baseband processor comprises a higher-layer processor configured to effect higher-layer processing of information processed by said baseband co-processor.

34. (Previously Presented) A timing synchronization method, comprising:

configuring a host baseband processor of a multi-mode device to operate in accordance with a first wireless communications protocol of a first wireless communications system;

configuring a baseband co-processor of a multi-mode device to operate in accordance with a second wireless communications protocol of a second wireless communications system; and

establishing, by said host baseband processor within said device, timing synchronization of said second wireless communications system to said first wireless communications system based on timing information transferred to said host baseband processor from said baseband co-processor, wherein said establishing includes issuing a timer capture interrupt to said baseband co-processor, and wherein said establishing comprises providing at least one timer value pertinent to a timing state of said second wireless communications system to said host baseband processor in response to issuance of said timer capture interrupt.

35. (Previously Presented) The method of claim 34, wherein said establishing includes reading a current value of at least one timer maintained by said baseband co-processor consistent with said second wireless communications protocol.

36. (Previously Presented) The method of claim 34, wherein said second wireless communications protocol comprises WCDMA, said establishing including storing at least one timer value and an additional timer value pertinent to an additional timing state of said second wireless communications system in first and second registers of said baseband co-processor.

37. (Previously Presented) The method of claim 34, wherein said host baseband processor is configured to effect higher-layer processing of information processed by said baseband co-processor.

38. (Previously Presented) A multi-mode wireless communication device, comprising:

a host baseband processor configured to operate in accordance with a first wireless communications protocol of a first wireless communications system; and

a baseband co-processor configured to operate in accordance with a second wireless communications protocol of a second wireless communications system,

wherein said host baseband processor is operable to time synchronize said second wireless communications system to said first wireless communications system based on timing information transferred to said host baseband processor from said baseband co-processor, wherein said host baseband processor comprises circuitry for issuing, from said host baseband processor, a timer capture interrupt to said baseband co-processor during a predetermined timer phase of said first wireless communications system, and wherein said baseband co-processor is configured to provide at least one timer value pertinent to a timing state of said second wireless communications system in response to issuance of said timer capture interrupt, said host baseband processor enables determining of a timing difference between said first and second wireless

communication systems based upon said predetermined timer phase and said at least one timer value.

39. (Previously Presented) The multi-mode communications device of claim 38, wherein said baseband co-processor comprises circuitry for reading a current value of at least one timer consistent with said second wireless communications protocol.

40. (Previously Presented) The multi-mode communications device of claim 38, wherein said host baseband processor comprises a higher-layer processing module and a modem for interfacing with said first wireless communication system, said higher-layer processing module being operatively coupled to said modem and to a baseband interface of said baseband co-processor.

41. (Previously Presented) The multi-mode communications device of claim 38, wherein said second wireless communications protocol comprises WCDMA, said baseband co-processor including first and second registers adapted to store said at least one timer value and an additional timer value pertinent to said second wireless communications protocol.

42. (Previously Presented) The multi-mode communications device of claim 41, wherein said at least one timer value corresponds to a slot counter and said additional timer value corresponds to a sample counter.

43. (Previously Presented) The multi-mode communications device of claim 38, wherein said host baseband processor comprises a higher-layer processor configured to effect higher-layer processing of information processed by said baseband co-processor.